AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (currently amended). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a~~n~~ first internal bus;

a send machine coupled between a host processor and the bus controller over a second internal bus; and

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus~~, the first FIFO not being coupled to the send machine over the internal bus~~.

Claim 2 (original). The computer system of claim 1, wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor.

Claim 3 (previously presented). The computer system of claim 1, wherein:

the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor; and

the send machine comprises means for transmitting the plurality of bytes over the system bus without interrupting the host processor.

Claim 4 (original). The computer system of claim 1, further comprising:

a receive machine coupled between the host processor and the bus controller; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller.

Claim 5 (previously presented). The computer system of claim 4, wherein the receive machine comprises means for generating a message checksum for a message while the message is being received by the bus controller over the system bus.

Claim 6 (previously presented). The computer system of claim 1, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device; and

retry means for attempting again to send the message over the system bus to the target device if it is determined that the message was not received without errors by the target device.

Claim 7 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device.

Claim 8 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device.

Claim 9 (previously presented). The computer system of claim 1, further comprising:

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Claim 10 (original). The computer system of claim 1, further comprising:

a byte timer coupled between the bus controller and the host processor.

Claim 11 (previously presented). The computer system of claim 10, wherein the byte timer comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 12 (currently amended). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus, the second FIFO not being coupled to the receive machine over the second internal bus but not over the system bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 13 (previously presented). The computer system of claim 12, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claims 14-41 (canceled).

Claim 42 (currently amended). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to ~~a~~ first internal bus;

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 43 (currently amended). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the system bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 44 (currently amended). A device for use in a computer system including a system bus and a bus controller coupled to the system bus and to a first internal bus and a second internal bus, the device comprising:

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine, the first FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.